CLAIMS

1. A tunable differential transconductor, comprising:

a tail current sink; and

a differentially-connected pair of FETs connected to said tail current sink, at least one of said FETs being a composite FET comprising a main FET and a switchable tuning element connected in parallel, said switchable tuning element operable to change an effective channel dimension of said composite FET.

2. The tunable differential transconductor of claim 1, in which the effective channel dimension is at least one of an effective channel width and an effective channel length.

3. The tunable differential transconductor of claim 1, in which:

said switchable tuning element comprises an auxiliary FET and a switch connected in series between drain and source of said main FET; and

said auxiliary FET comprises a gate connected to the gate of said main FET.

4. The tunable differential transconductor of claim 3, in which said switch comprises a control input connected to receive a tuning control signal.

5. The tunable differential transconductor of claim 3, in which:

said switch comprises an FET; and

said control input comprises the gate of said FET.

6. The tunable differential transconductor of claim 1, in which said switchable tuning element comprises series circuits connected in parallel between source and drain of said main FET, each of said series circuits comprising an auxiliary FET and a switch connected in series, said auxiliary FET comprising a gate connected to the gate of said main FET.

7. The tunable differential transconductor of claim 6, in which said switch comprises a control input connected to receive a tuning control signal element.

8. The tunable differential transconductor of claim 7, additionally comprising a switched control device, said switched control device comprising:

an input connected to receive said control signal; and

outputs connected to deliver said tuning control signal elements to said control inputs of said switches of said series circuits.

9. The tunable differential transconductor of claim 7, in which:

said switch comprises an FET; and

said control input comprises the gate of said FET.

10. The tunable differential transconductor of claim 6, in which said series circuit comprise said auxiliary FETs of different channel dimensions.

11. The tunable differential transconductor of claim 10, in which said auxiliary FETs have channel widths equal to the channel width of said main FET divided by different integers.

12. The tunable differential transconductor of claim 10, in which said auxiliary FETs have channel widths equal to multiples of the channel width of said main FET.

13. The tunable differential transconductor of claim 1, in which both of said FETs are composite FETs each comprising a switchable tuning element connected in parallel with a respective main FET.

14. A method for tuning a differential transconductor, the method comprising:

providing said differential transconductor comprising a tail current sink and a differentially-connected pair of composite FETs connected to said tail current sink, said composite FET each having an effective channel dimension; and

changing said effective channel dimension of at least one of said composite FET to establish at least one of (a) a desired transconductance, (b) a desired transconductance linearity, and (c) a desired offset of said differential transconductor.

15. The method of claim 14, in which said effective channel dimension comprises at least one of effective channel width and effective channel length.

16. The method of claim 14, in which said changing establishes said desired transconductance, and comprises:

applying a calibration input voltage to said differential transconductor;

measuring an output current of said differential transconductor; and

changing said effective channel dimension of said composite FET to change said output current to a value corresponding to the product of said desired transconductance and said calibration input voltage.

17. The method of claim 16, additionally comprising adjusting said tail current to tune said desired transconductance.

18. The method of claim 14, additionally comprising adjusting said tail current to tune said desired transconductance.

19. The method of claim 14, in which:

said method additionally comprises:

setting said effective channel dimension to an initial channel dimension, and

adjusting said tail current to establish said desired transconductance; and

said changing comprises:

measuring a turn-on voltage of said composite FET, and

changing said effective channel dimension to set said turn-on voltage equal to a desired turn-on voltage commensurate with said desired transconductance linearity.

20. The method of claim 19, in which said initial channel dimension is a maximum effective channel dimension.

21. The method of claim 19, in which said adjusting comprises using a replica bias method.

22. The method of claim 19, in which said adjusting comprises:

applying a calibration input voltage to said differential transconductor;

measuring an output current of said differential transconductor; and

adjusting said tail current to change said output current to a value corresponding to the product of said desired transconductance and said calibration input voltage

23. The method of claim 22, in which said adjusting comprises using a replica bias method.

24. The method of claim 19, in which at least one of said setting, said adjusting, said measuring and said changing is performed on a replica of said differential transconductor.